DBBC: Status Report

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A complete DBBC unit is in these days in the final assembly stage and it will be showed at the coming 4th IVS General Meeting to be held in Conception in January. The system is composed by four IF units (ConditioningModule), a digital system clock generator (CaTModule), four samplers (ADBoard), two in-out units (FiLaBoard), and a set of eight-sixteen processing units (CoreModule). Some delay in the Core boards is due to the delivery time of the main FPGA devices from Xilinx.

MPI developed the ADBoard that has been successfully tested in the functionality. CoreModule has been developed in IRA specifically for the project and a version is today produced with enhanced performance. The CaT unit from IRA is still in a not final version and will be realized in the Core format. FiLa boards, developed in IRA are VSI compatible only and includes DA monitoring features. ConditioningModules developed in IRA support a 3 GHz bandwidth in portions of band variable with selectable filters. Not all the filters are still realized.

Different configurations are today operative for a set of four bandwidths ranging from 250 KHz to 16 MHz, with 256 MHz input bands spanned from 1 MHz to 2.048 GHz. Output of these configurations is for two VSI units at a total data rate of 2.048 Gbit/s.

Other configurations are in development for 512 MHz input bands and different performance such as multi-channels and wide band channels.

Starting with 2006 a multi-step process will be necessary for testing the unit, develop new configurations, improve the performance with a new class of FPGA device, today under test. Moreover a second unit will be built for performing digital-digital testing. Additional stage of the project will take into consideration optional units for RFI mitigation and IF sampled transportation.