RDBE: 2nd Generation VLBI Digital Backend System

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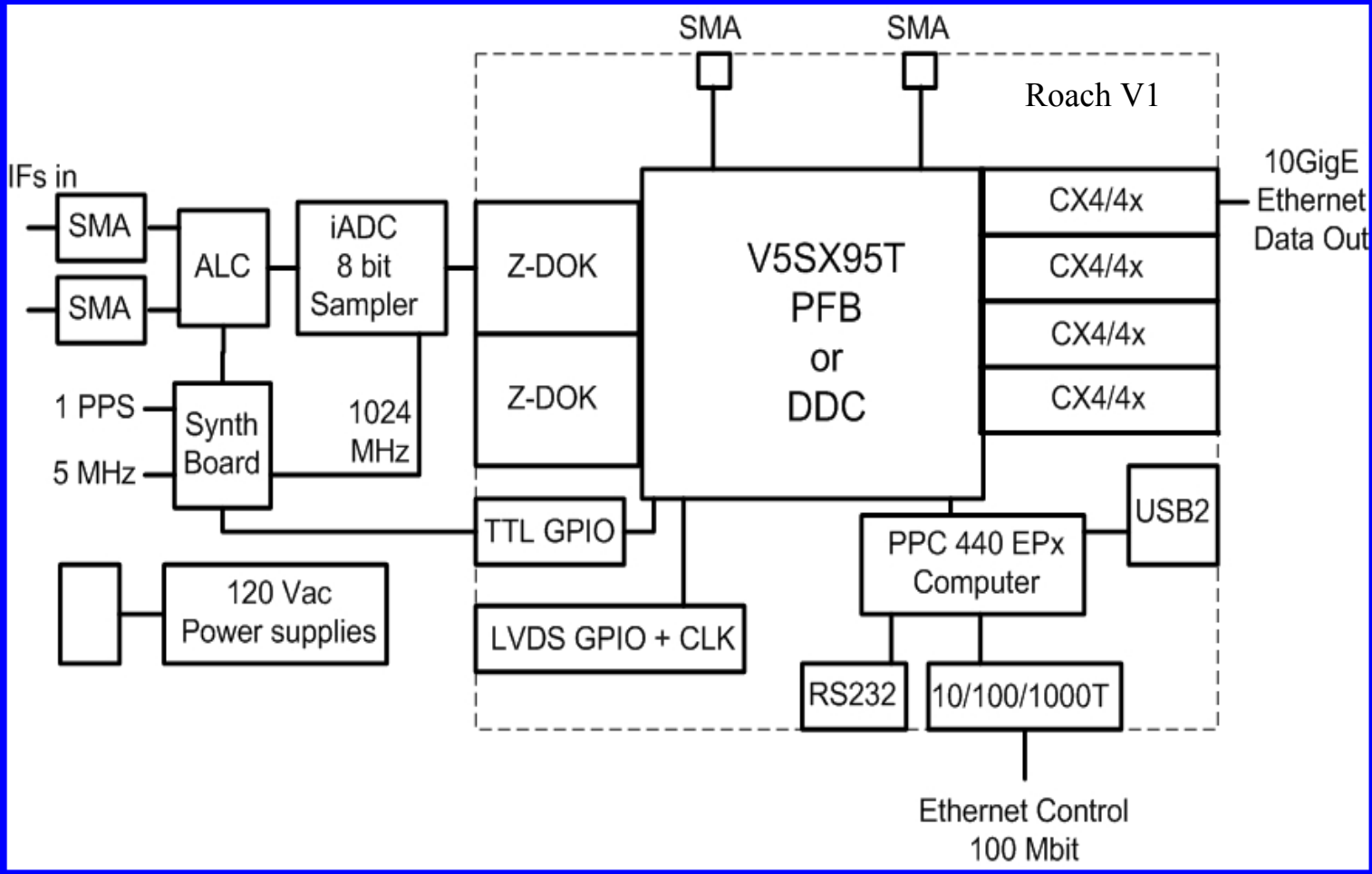
1st generation DBE development at Haystack

- DBE1 (developed 2004-2006)
  - Hardware is based on a flexible FPGA-based signal-processing board from UC Berkeley ("iBOB")
  - Developed collaboratively between Haystack and UC Berkeley Space Sciences Laboratory
  - DBE design based on Polyphase Filter Bank (PFB) concept
  - Processes each of 2x512MHz IFs to 16 32MHz subbands on two VSI-H output connectors; total 4096Mbps to 2xMark 5B+
  - Sample-clock synthesizer with temp coef <1ps/degC
  - In regular use for past ~3 years for mm-VLBI experiments and VLBI2010 development; often used with two systems in parallel (i.e. 2 DBE1s driving 4 Mark5 B+'s) for sustained 8Gbps recording rate

2nd generation: RDBE

- Based on ROACH board developed by Berkeley, NRAO and South Africa
- Up to 10 GigE data output(s) to Mark 5C/Mark 6
- Collaborative firmware/software development by Haystack, NRAO, Berkeley and South Africa
- Haystack developing system-level FPGA framework, PFB signal-processing module, and software framework
- NRAO creating tunable DDC version to replace analog BBCs; part of VLBA upgrade to 4Gbps
- PowerPC OS developed by South Africa

ROACH block diagram



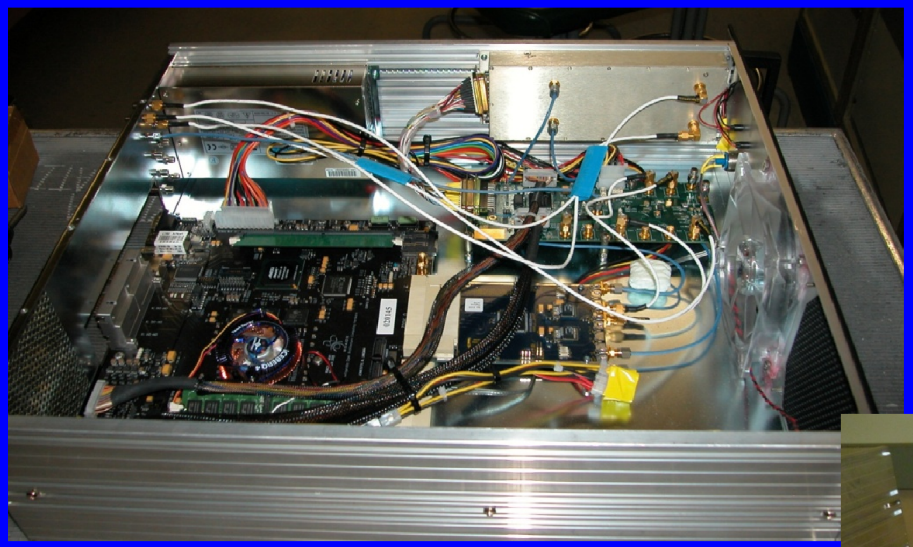
RDBE characteristics

- Common FPGA, OS and software framework
  - VSI-S compatible control/monitor
  - Continuous state-count monitoring
  - T_{sys} measurements using synchronously-controlled noise diode
  - Multiple-channel real-time phase-calibration extraction
  - RDBE/DDC personality is software changeable (few seconds)
- Two hardware variants (both with ROACH board)
  - RDBE-H
    - Single ADC board (i.e. 2 IF inputs)
    - IF auto-level control (ALC) using external digitally controlled attenuator
    - NRAO-designed synthesizer board (4 sampler clock outputs, four 1pps outputs
  - RDBE-S
    - Dual ADC boards (i.e. 4 IF inputs)
    - Haystack-designed synthesizer board (1 sample clock output, single 1pps output)

Three Initial Designs with Common Software Architecture

- RDBE-H hardware platform
  - Target: VLBI2010 geodesy
    - IF Inputs: 2x512 MHz
    - Output: 16 arbitrarily selectable 32MHz PFB channels (2 Gbps total on single 10GigE output); VDIF data format
    - Other: ALC board for control of IF input power; Tsys; phase-cal extraction
    - Status: Tsys & pcal extraction still under development/test
    - Plans: Extend to 4x512 MHz IF inputs (4 Gbps output rate)
  - Target: VLBA
    - IF Inputs: 2x512 MHz
    - Output: 8 sub-bands, each selectable from either IF input, and each with selectable BW from 62.5 kHz to 128 MHz; frequency step-size TBD (multiple of 15.625kHz?)
    - Same as above, except flexible Digital-DownConverter (DDC) module replaces PFB module
    - Status: Under test at NRAO
- RDBE-S hardware platform
  - Target: Wideband astronomy
    - IF Inputs: 4 x 512 MHz
    - Outputs: 4 x 512 MHz bands – 2 b/s; 8Gbps total on four 10GigE outputs; VDIF data format
    - Status: Occasional duplicate samples (under investigation)

RDBE housed in 3U ‘ROACH Hotel’

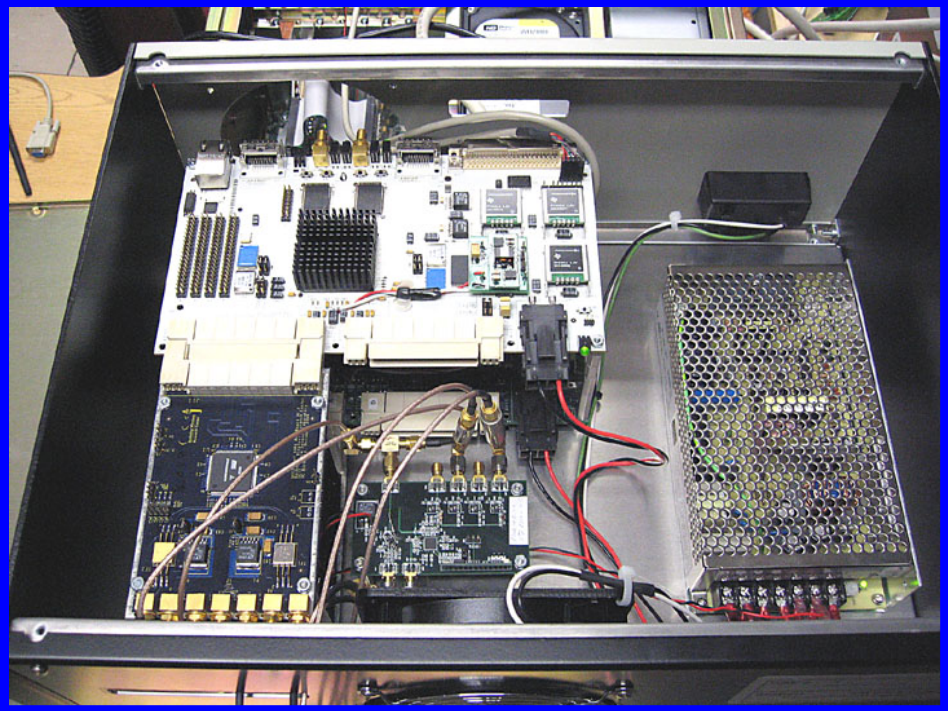


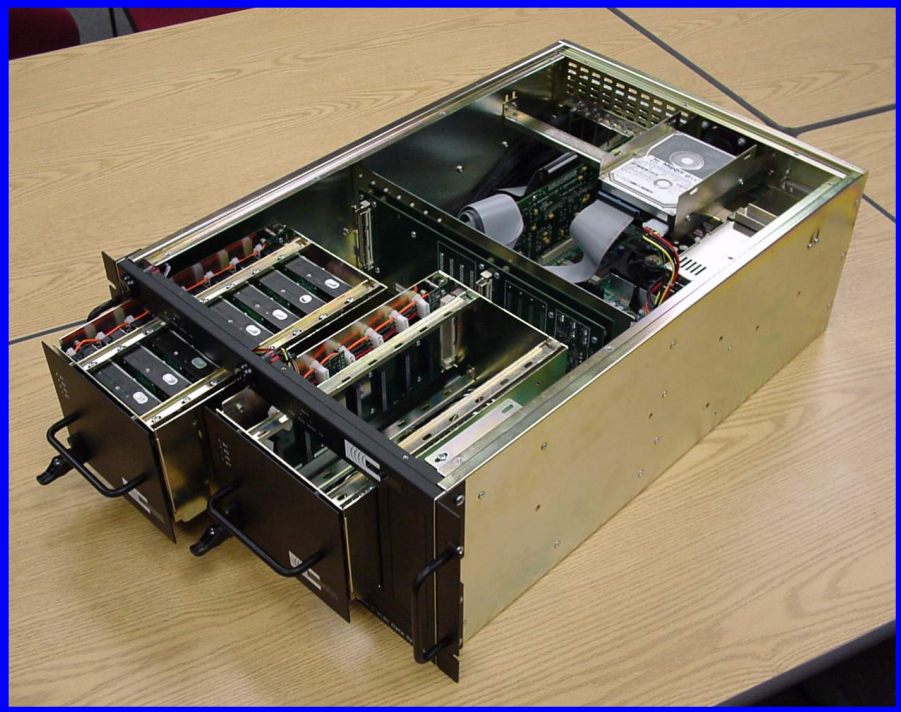
Summary

- 3 RDBE versions under development; all expected to be operational with next few months
- Hardware can be purchased from Digi-Comm Electronics,
  Richmond, CA

Questions?

DBE System



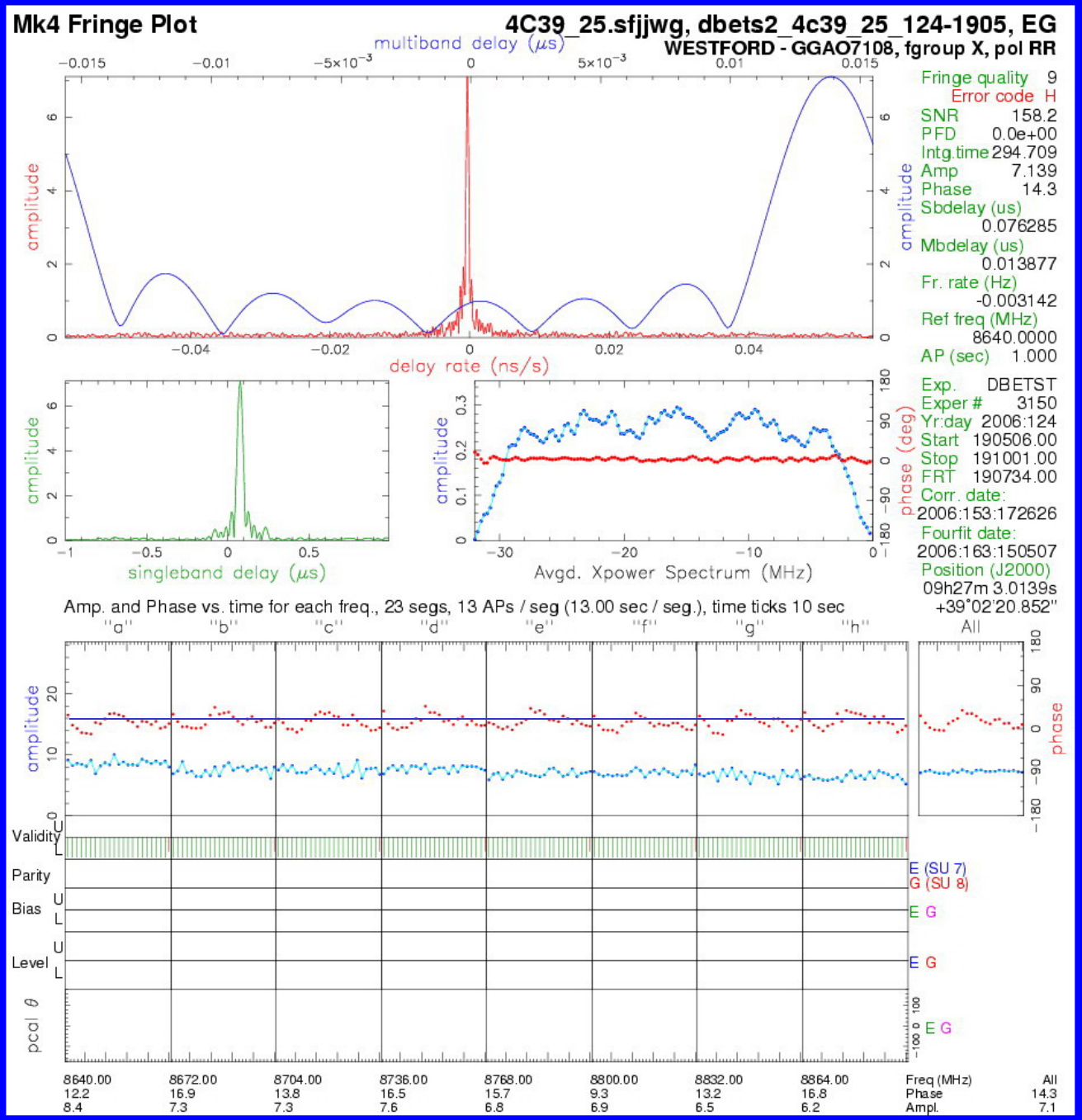


DBE: 2x (iADC + iBOB);
8Gbps output (4xVSI-H)

Mark5B+: 2Gb/s VSI-H each
(DBE supports 4 Mk5B+s)

- DBE Total system cost ~$65K

Current modes: 15 channels, each 32MHz, 2-bit = 1920Mb/s
15 channels, each 16MHz, 2-bit = 960Mb/s



DBE1 vs DBE1 with no phase adjustments whatever

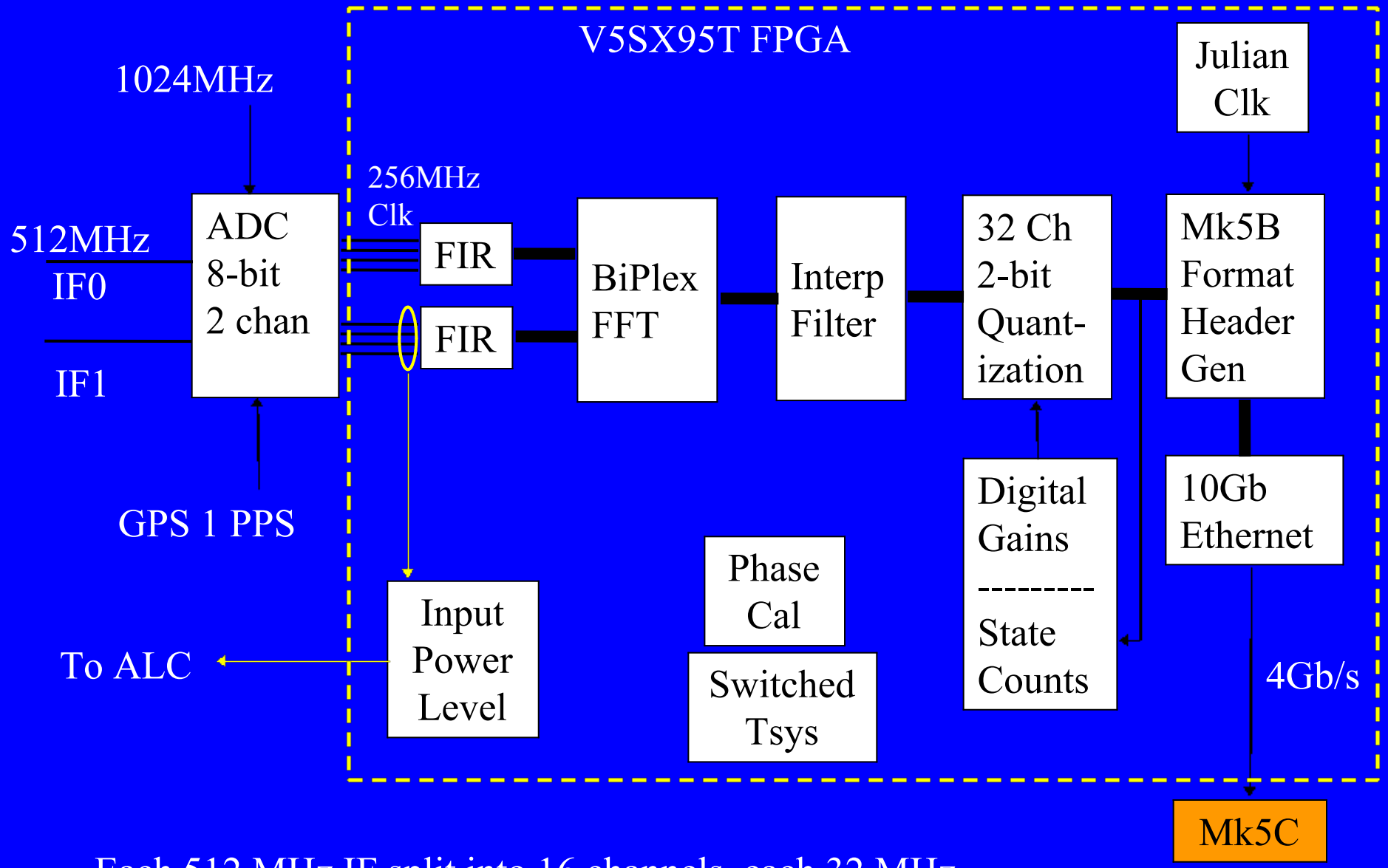
RMS phase across frequency channels:

RMS: 2.5 deg

Theor: 1.0 deg

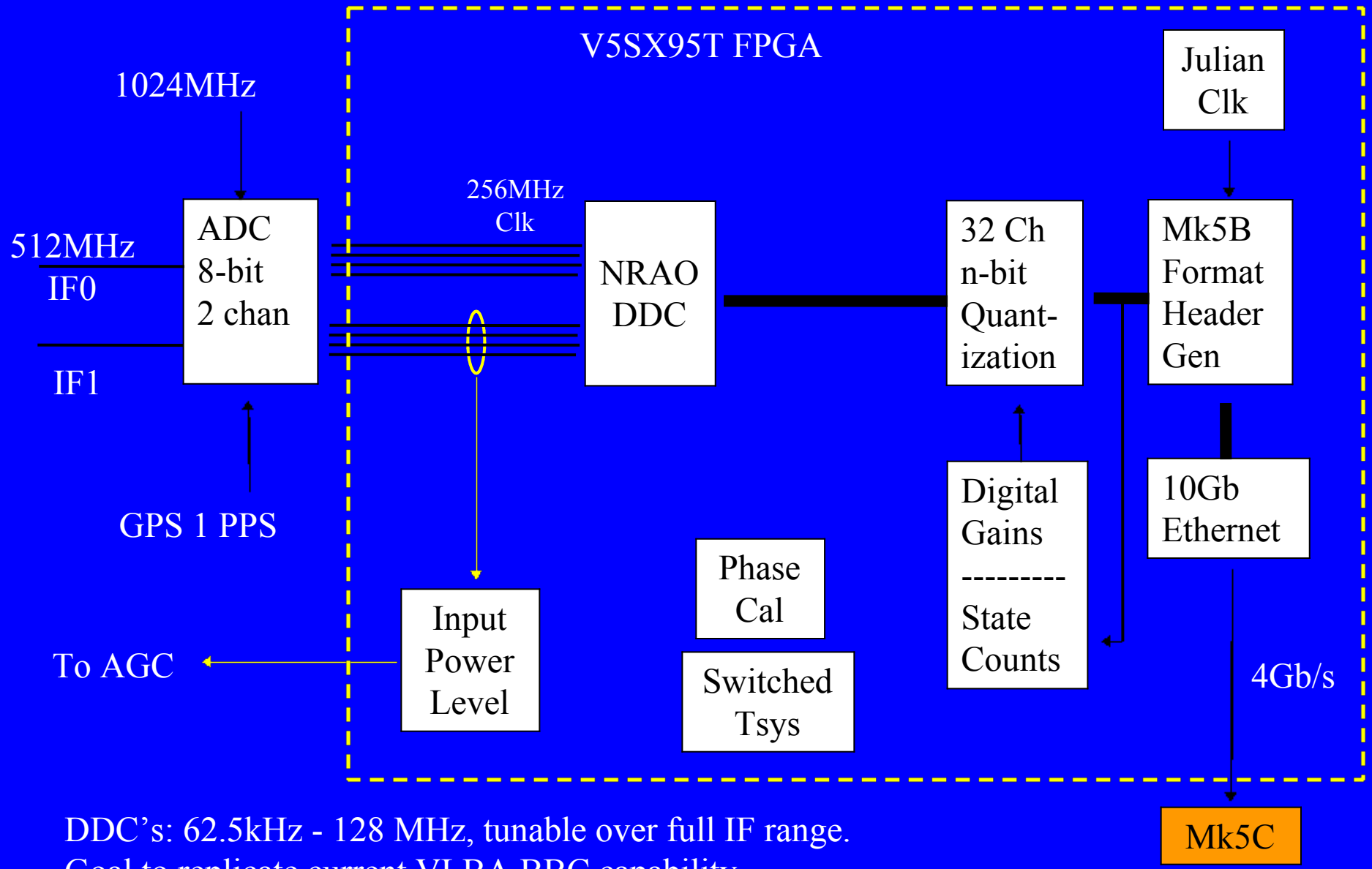
Comparable to best we've seen even with 'manual' adjustments to embedded phase-cal

RDBE diagram (PFB mode)



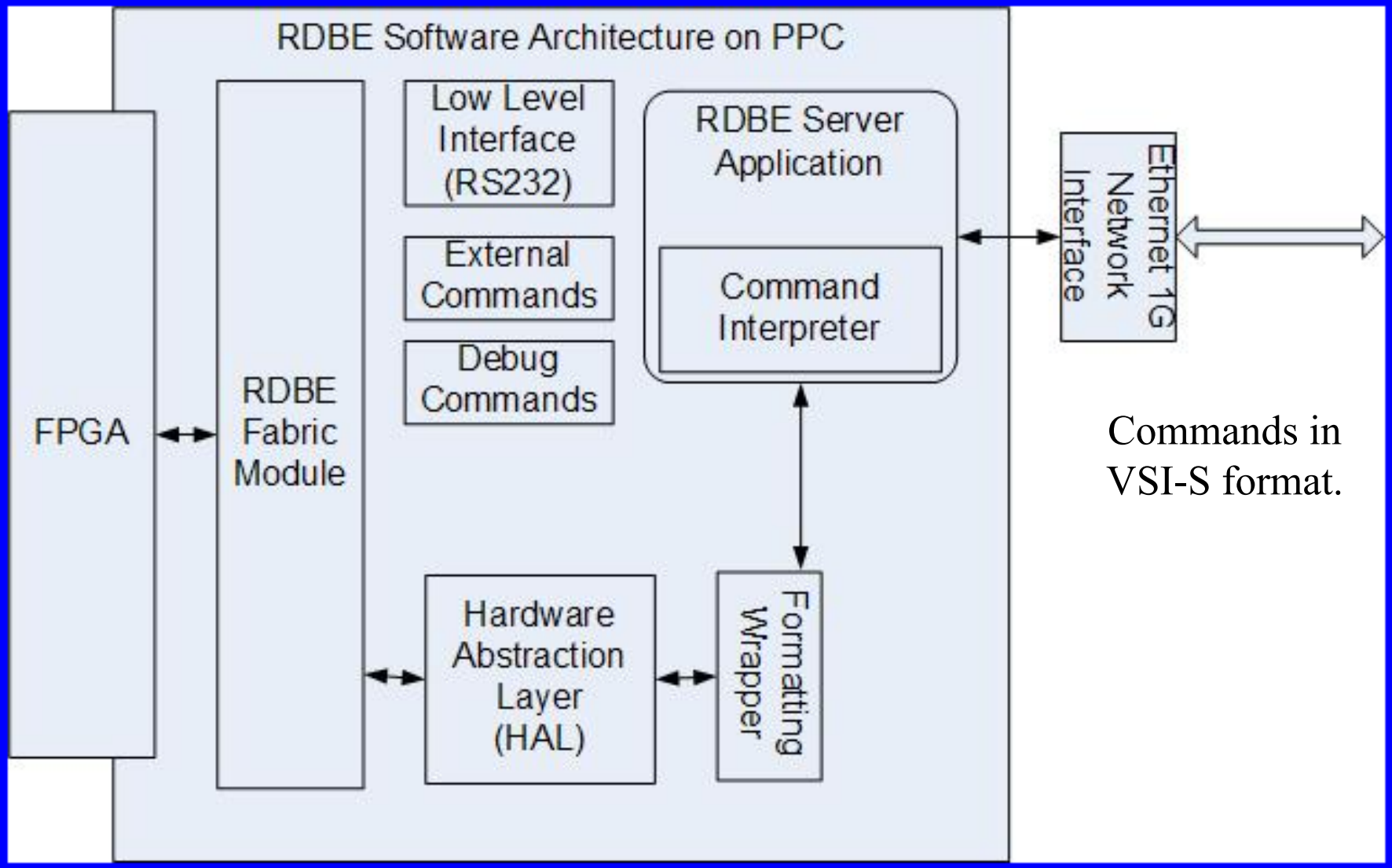
Each 512 MHz IF split into 16 channels, each 32 MHz.

RDBE diagram (DDC mode)



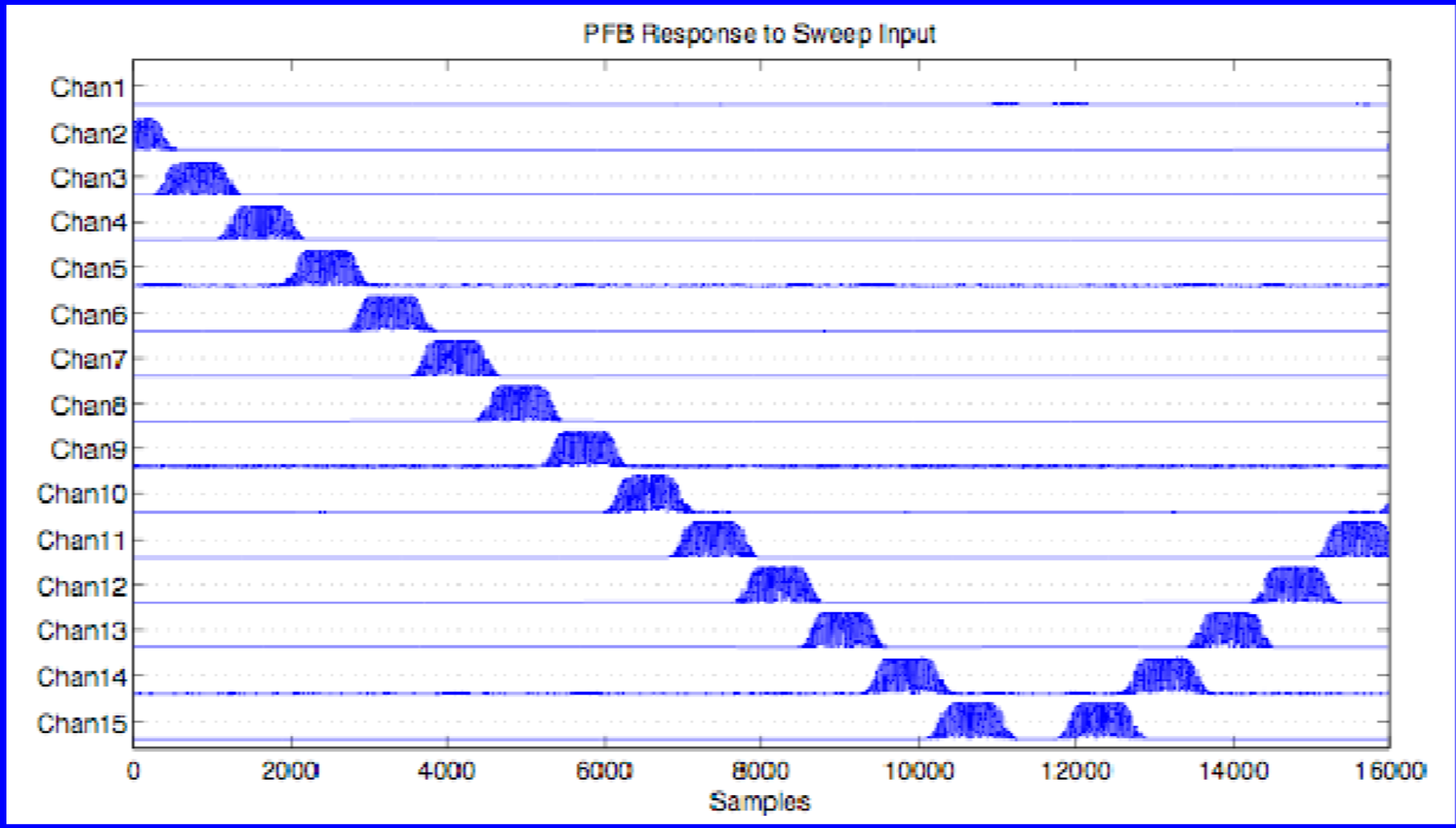
DDC's: 62.5kHz - 128 MHz, tunable over full IF range.
Goal to replicate current VLBA BBC capability.

RDBE Software Architecture



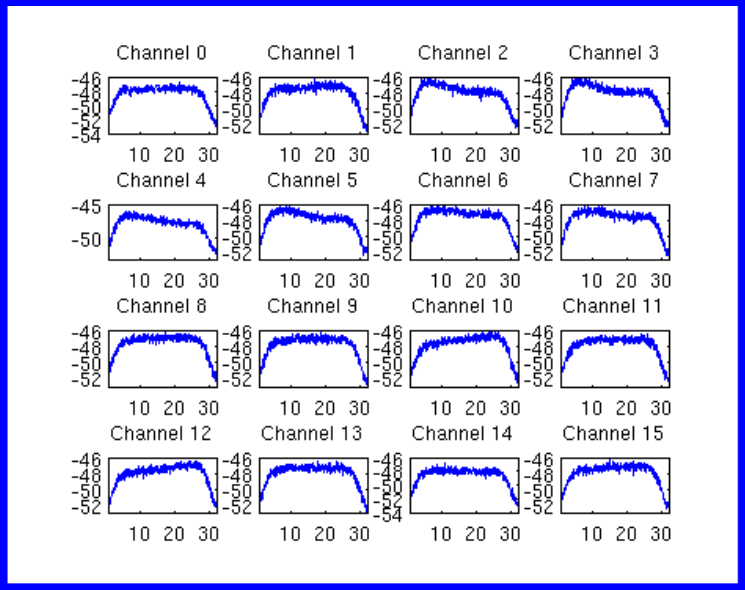
Commands in VSI-S format.

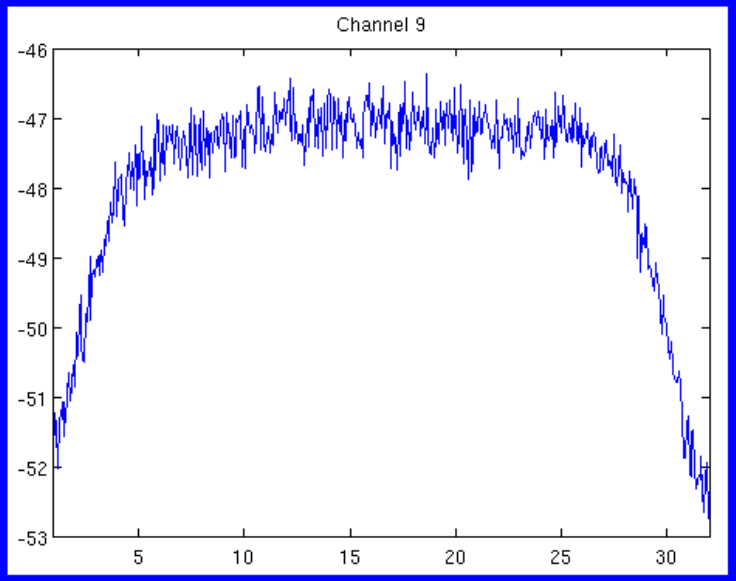
Sweep Through PFB Channels

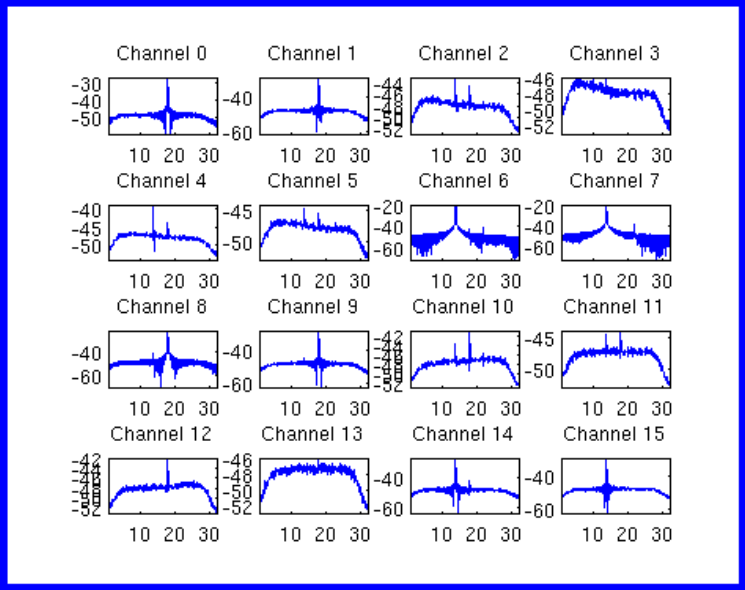


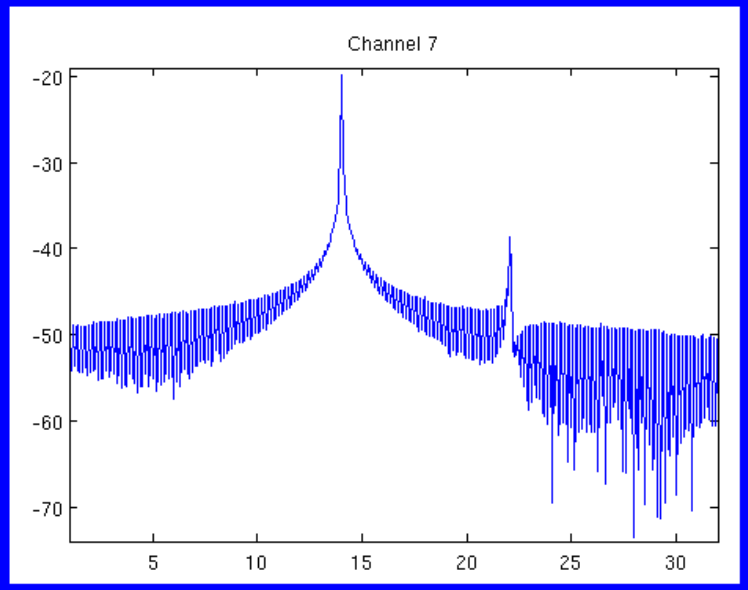
10GbE data output processed in MATLAB

Noise and Tone Testing









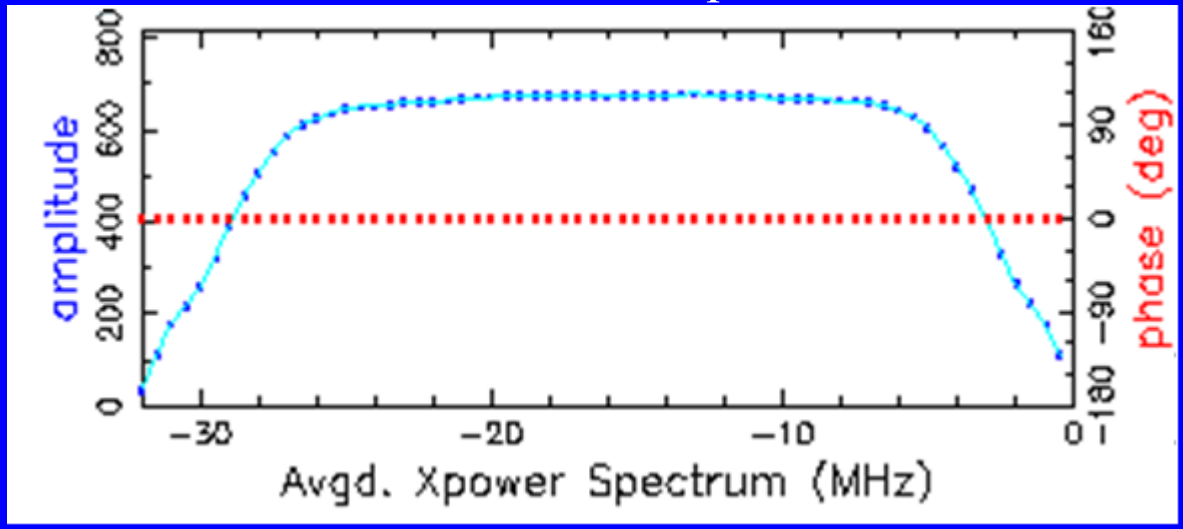
10GbE data output processed in MATLAB. Testing by Spencer Cappallo

RDBE VLBI Demonstration

- Stations
  - Westford 18m
  - MV3 5m at GGAO
- Source 4C39.25
  - 10 minute scan
- Cooled broadband dual linear polarization feed and LNAs covering 2-12 GHz
  - 512 MHz band selected around 8.5 GHz
- RDBE at both sites
  - Eight 32-MHz channels from each of two polarizations merged onto single 10GigE line at 2 Gbps
  - Data recorded on Mark5C in Mark5B data format
- Processed on Haystack Mark4 correlator

VLBI Results from RDBE test

Autocorrelation Spectrum



Amp & Phase vs time on Westford-to-MV3 baseline (SNR~20)