Haystack DBE Program

Dan Smythe
Sheperd Doeleman
MIT Haystack Observatory

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What we are doing

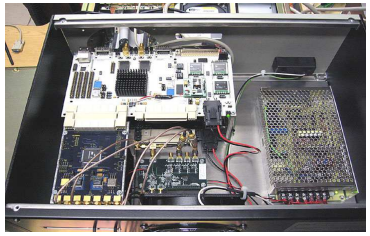
- Developing DBEs with NSF grant in collaboration with Berkeley Space Sciences Laboratory (SSL)
- 4Gbps VLBI experiments planned with DBE and Mark5B+ under UVLBI grant

Haystack DBE Status

- 2 Gbps prototype units constructed, tested and used for VLBI at 1 Gbps with Mark 5B (sign bits only)
- 4 Gbps prototype will be VLBI-tested in January 2007 in cm-wavelength tests on Westford-GGAO baseline
- Single chassis contains two DBE boards $\rightarrow$ 8 Gbps on four VSI-H outputs;
  direct cost ~$15K
- Can be reconfigured to support 3-6 DBBC's per DBE board (Not Yet Implemented)
- Flexible IF/LO system being built to accommodate 100MHz to 15GHz input IF
- Plan to utilize 10GigE output for VLBI data output
- In discussions with NRAO about developing next-generation DBE FPGA board

DBE Development

- FPGA-boards in collaboration with Berkeley/SSL
- Polyphase filter bank, VSI interface
- Integrated with Mark 5B data system
- Specifications:
  Sampling: 2x512 MHz bandwidth
  Output: (2x) 16 2-bit sampled 32-MHz channels
  Data rate: 4 Gbps on 2 VSI-H outputs



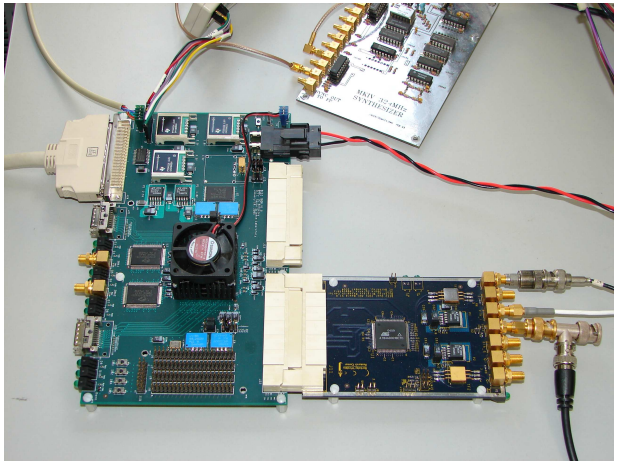
Proposal History

- Fall 2004: initial collaboration between Berkeley SSL and Haystack on DBE.
  - SSL Hardware: ADC, iBOB, BEE2
  - iBOB (single FPGA) able to meet DBE specs.
  - Algorithm work on DSP necessary for VLBI.
  - Haystack contributes to hardware/firmware work at SSL.
- Jan 2005: DBE proposal submitted to NSF.
- Apr 2006: DBE grant received.

Rationale

- FPGA-based architecture
  - A future path for many applications:
    Spectrometers, receivers, filters, array correlators, etc.
- Advantages:
  - Reliability
  - Absolute repeatability
  - Absolute stability
  - Low cost

DBE/iBOB+ADC



Tests with DBE Prototypes

- Mark 5B bit mask set to record only sign bits to reduce data rate to1Gbps for Mark 5B recording
- Zero baseline tests w/o and w/ rate offset
- 230GHz VLBI between SMTO and SMA/CSO
- X-band observation between Westford-GGAO
  - successful test with simultaneous Mark 4 -> Mark 5A and DBE -> Mark 5B recordings
  - Excellent agreement between Mark 4 and DBE fringes
  - SBD and MBD for DBE fringes agree to within ambiguity: consequence of PFB
- Field system running on Mark5B, channel gains set manually via serial link from Mark5B to DBE

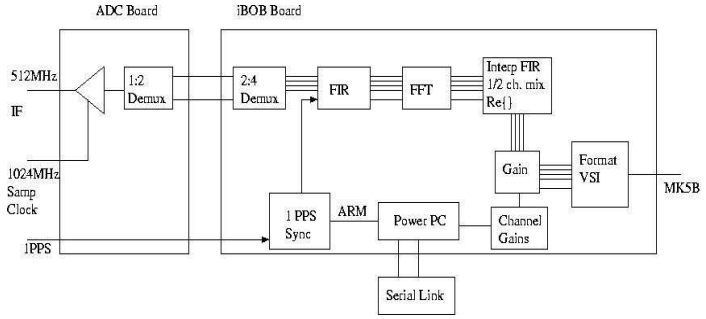
2.5-Year Plan

- Firmware:
  - State Count level correction on-board DBE;
    possibly done on Mark5B with serial feedback.
  - Optimize Filter shapes (increase FIR/Interpolator taps).
  - 10GigE protocol and output for compatibility with COTs NICs and RAID arrays.
  - Pulsar gating capability.
  - Digital Downconverter implementation for spectral line applications.
- Hardware:
  - Flexible IF/LO system: input is 100MHz to 15GHz,
    output is filtered 512MHz band. ($7.5-10K)
  - Decision on re-spin of iBOB for VLBI-specific application: NRAO collaboration?
  - Final Chassis build.
- Software:
  - Control software integration.
  - Solution to DBE mode switching.

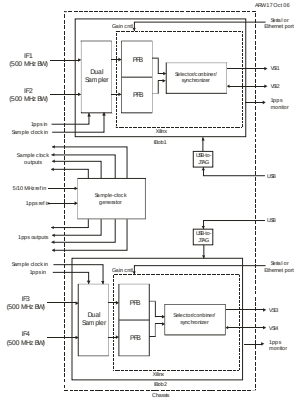
Future

- SSL has 3-year ATI grant to continue general purpose FPGA development for Radio Astronomy.
- Virtex 5-based hardware within 3 years with corresponding firmware libraries.
- ADC will have 3 GSamp/sec A-to-D with 6 GSamp/sec interleave mode.

Prototype DBE Architecture



DBE Block Diagram



Flexible IF/LO System